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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2891
Examiner: Dana Farahani
Confirmation no.: 5973

In Re PATENT APPLICATION Of:

Applicant:	Noriyuki Miura	)
Serial No.:	10/690,579	)
Filed:	October 23, 2003	) REQUEST FOR
For:	SEMICONDUCTOR DEVICE AND METAL-OXIDE SEMICONDUCTOR FIELD-EFFECT TRANSISTOR	) RECONSIDERATION
Attny Ref.:	MAE 296	)

January 2, 2006

MAIL STOP AFTER FINAL RESPONSE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

As suggested by SPE Bill Baumeister at the personal interview of November 22, 2005, the Applicant requests reconsideration.

This paper is in response to the Official Action mailed on August 8, 2005. A Notice of Appeal was filed on November 8, 2005. No fee is due. However, please charge our Deposit Account No. 18-0002 if any fees are needed to enter this paper, and please advise us accordingly. It is noted that no petition is required because of the authorization to charge, but please consider this paper a petition for extension of time if needed.

The Examiner's consideration of the following arguments is requested:

Claim 2. Claims 2, 3, 10, and 11 were rejected under §103(a) as being unpatentable over Bulucea and Chen in view of Tsukii '858, previously applied. With respect, the asserted combination is not suggested because the secondary references are not concerned with the same sort of device as is the primary reference, Bulucea. Bulucea discloses a device made with similar polarity materials (for example, an n++/n/n++ device) while the other two disclose only n/p or p/n junction devices (e.g., n/p/n or p/n/p transistors).

Bulucea presents a detailed description and exhaustive explanation of its device, which inherently teaches away from adding features from other references, especially when the other references are not directly relevant and teach only vaguely in regard to the structure, which is respectfully submitted to be the situation in this case.[1]

Chen in fact does not disclose any specific devices at all, only a substrate on which devices are to be formed by "conventional CMOS processing" (col. 6, line 45), a phrase which is seen to imply n/p/n or p/n/p devices. Furthermore, Chen's substrate processing does not take place in any region where the conventional devices are formed (col. 6, lines 38-43), and therefore Chen's lengthy disclosure relating to its object of forming gettering regions (col. 2, lines 4-12) is irrelevant to forming active devices; thus, it is irrelevant to claims 1 and 2, which recite

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[1] It was previously argued:

"The doping scheme of Fig. 2, which creates a pn junction, is important to Bulucea's theory and to the transistor shown in applied Fig. 16. Starting at col. 13, line 18, Bulucea explains in detail how this structure works. For example, col. 14, line 34, explains that "y_{JMIN} is the thickness of the channel-side portion of the depletion region 44 ... and thus is the minimum junction depth for buried-channel operation. In order to determine channel-side channel/body depletion thickness y_{JMIN}, the center dopant profile of FIG. 2 is ... at uniform value N_B across ... body region 22." The dopant quantity N_B occurs in equations 9, 10, 24, 25, 29, 34-40, 42, 44, 46, 49, 50-51 (as an averaged quantity N_B^{-m}, see col. 9, line 58), and 69, and also in the un-numbered equation in claim 13. The related quantity N_{B0} (background dopant concentration, see col. 9, line 55) appears in several other equations.

"Clearly, the doping N_B of the region 22 is an important aspect of the theory and construction of Bulucea's Fig. 16 transistor. Figs. 15-16 , which show the preferred embodiment, and come directly after the theoretical section of the description and embody that theory.

"By disclosing that the underlying layers 106, 166 of Fig. 16 are important to the functioning of its invention, Bulucea inherently teaches against removing them, altering them, or interposing anything between them and the upper layers (such as an un-doped silicon layer that would destroy the pn junction Bulucea has so carefully calculated)."

specific device features. With respect, nothing in Chen other than the bare phrase "conventional CMOS processing" relates to the instant subject matter.

Similarly, there is nothing to suggest that Chen be combined with Bulucea. The primary reference discloses detailed and specific active device structures, while Chen discloses nothing about forming active devices, and the gettering which Chen does disclose would be of no use to Bulucea.

If Bulucea were subjected to the gettering of Chen, then the doping might be affected, because Chen's gettering removes metals (col. 6, line 4) and semiconductors, which are close to metals in their properties, might also be removed. Any change to the doping of the layers 102 and 104 would not only interfere with intended action at the interface with the p and n regions 106 and 166 (Fig. 16) but also with the intended conduction from the lower contact layer 124, which serves as an electrode (col. 35, line 32).

Therefore, the person of ordinary skill would not have combined Chen with Bulucea.

The previous arguments are respectfully reiterated.[2]

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[2] It was previously argued:

"Chen is applied for teaching the addition of the SOI layer that is lacking in Bulucea. The Examiner states that the SOI layer would prevent electrical interference from adjacent devices (page 3, line 1).

"However, Bulucea *already* has an insulator to separate and isolate the transistors, namely, field-oxide region 108 which "separates the device region for CJIGFET 100 from other such active device regions" (col. 35, line 8). With respect, Bulucea needs no other insulation layer to prevent interference, contrary to the motivation proposed by the Examiner.

"The Opposite of Insulation. Furthermore, no insulating layer is provided anywhere *under* the applied transistor of Bulucea. The layer 124 of Fig. 16 is metallic (col. 38, line 59). Thus, in the region under the channel, Bulucea provides not an insulating layer, but the opposite—a metallic conducting layer.

"There Is No Expectation of Success. Chen discloses that its uppermost SOI layer 16 is the portion in which IC devices will be formed (col. 3, line 20), but there is no explanation whatsoever of what the IC devices are or how they are formed. Chen is concerned only with gettering to remove metals from the SOI (col. 1, lines 28-43; col. 5, lines 33-40), which appears to the Applicant to be a step prior to forming any ICs. The region under the gate electrode 20 and gate stack 22 is shielded, and is not gettered."

Tsukii is relied upon for disclosing a density of carriers per cubic centimeter at col. 7, lines 27-33. Tsukii discloses a channel carrier concentration of 2×10^{17} cm^{-3} but does not disclose whether this concentration is in an n-type or in a p-type channel. Neither is there any indication that the claimed n++/n/n++ structure is used by Tsukii, and therefore its teachings about carrier concentration are not germane to Bulucea, and the person of ordinary skill would not have substituted this concentration into the carefully-designed structure of Bulucea.

Thus, the teachings of Chen and Tsukii are not relevant to the structure of Bulucea, and therefore these references should not have been combined. The earlier arguments regarding Tsukii are respectfully reiterated.[3]

Claim 7. Claims 7, 8, 15, and 16 were rejected under §103(a) as being unpatentable over Bulucea and Chen in view of Kato '678, previously applied. This rejection is respectfully traversed. Claims 7 and 15 recite channel length.

(1) Kato states that the 0.15 μm length disclosed at col. 2, line 5 (applied in the rejection) makes it "difficult that the high integration memory device of 256 mega bits or more be realized" (col. 2, line 6). Thus, Kato teaches *away* from using this length and the person of ordinary skill in the art would never have combined the references based on this teaching.

(2) Bulucea is greatly concerned with channel depth, but completely ignores channel *length*; all of its figures show channel cross sections, and no variable for channel length appears in its long list of variables (col. 9, line 31 to col. 11, line 35). Why?

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[3] It was previously argued:

"(1) The Examiner asserts obviousness based on making Bulucea's structure applicable in an integrated circuit structure like that of Tsukii. This is respectfully traversed on the basis that Bulucea *already* shows an integrated circuit in applied Fig. 16, with complementary n-p and p-n transistors formed on a single substrate. (Two transistors on one substrate is believed to define an integrated circuit.) The asserted motivation is, with respect, obviated.

"(2) Furthermore, Bulucea goes to great lengths to calculate based on an optimum channel doping concentration N_C (col. 9, line 60). Concentration N_C appears in equations 9-11, 16, 17, 19, 20, 22, 24, 25, etc. The person of ordinary skill would not have throw away Bulucea's carefully and fully theorized values of N_C due to the mere mention of some other concentration in a reference like Tsukii, that is not directly related to Bulucea's structure and does not contain any explicit teaching of the advantage of its particular concentration."

The Applicant believes that Bulucea is aware that the properties of its structure can be extended to a desired length, knows that the person skilled in the art would also be aware of this, and therefore provides no discussion of the length. An electrical analogy to Bulucea would be a theoretical discussion of a coaxial cable structure given and discussed only in cross section; the properties of any length of such coaxial cable would evident to the person skilled in the art of coaxial cables.

Thus, any teaching of Kato about length is seen to be irrelevant to the teachings of Bulucea, and therefore combination is not suggested.

Claims 10 and 15. Claims 10 and 15, depending from claim 9, are analogous to claims 2 and 7 dependent from claim 1. The same arguments set out above apply equally to claims 10 and 15 as to claims 2 and 7. Reconsideration is requested, especially for these claims.

Respectfully submitted,

January 2, 2006
Date

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I certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office (fax no. 703-872-9306) on January 2, 2006.

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